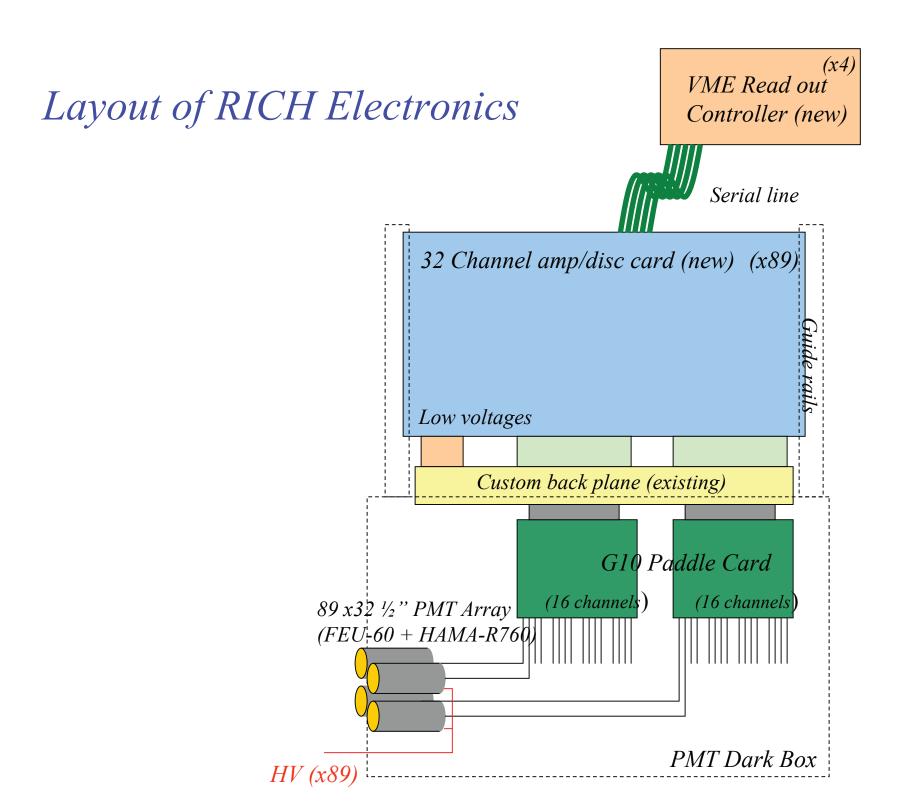
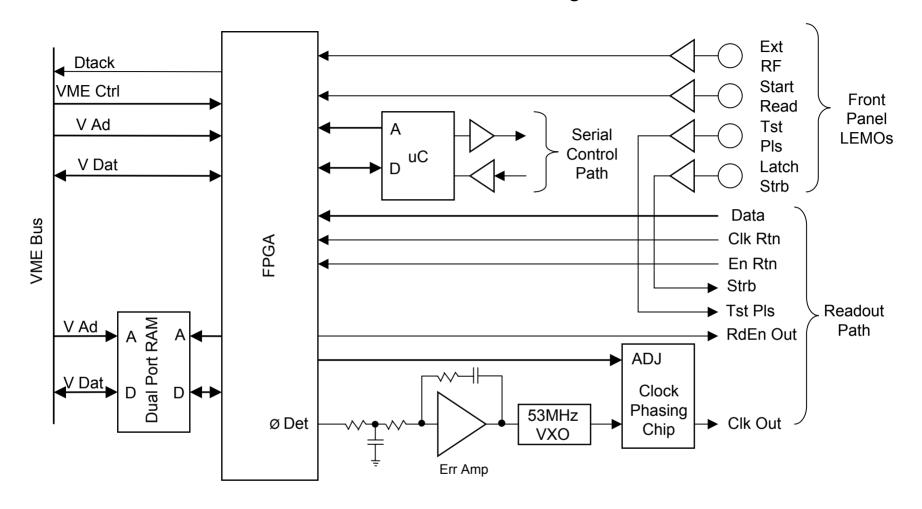
RICH Update

Mark Messier (for Sten Hansen, Andre Lebedev, and Sharon Seun) MIPP Collaboration Meeting 10 August 2002 FNAL

- Electronics Status
- HV
- Monte Carlo



907 RICH Readout Card Block Diagram



E907 RICH Electronics Status

Parts for prototypes are here

Layout for 32 channel card finished

I need to check the layout. We can presumably get PC fab quotes this coming week, and have Harvard bankroll the order as with the readout cards.

5 Readout cards are here and 1 is assembled

Engineering co-op is writing equations for readout card fpga (another week probably)

Terry Kiper has not yet started on uC code for readout card or 32 chan cards, but he can begin soon (this week perhaps)

The programming effort is 2-3 weeks of work including both cards

If we do things correctly, we will finish the readout card firmware about the time the 32 channel cards arrive. A list of ongoing tasks that relate to the E907 RICH boards:

32 channel card:

Prototype design, schematic drawing and PC layout is complete. Parts for the prototypes are on hand.

Assembly of 2 prototype cards: 1 week in Bob Jones' tech shop.

Bench testing/debugging of prototypes: 1 week.

In situ testing on RICH: 3 days.

Preparation of parts orders for production quantities: 2 days

Assume contract for board fab, assembly and testing is done by Harvard.

Readout card:

5 prototype cards are here, 1 is 90% assembled (we are missing a couple of LVDS chips).

Logic chip equations: 40% complete, another week to complete.

If the present iteration of the board works with few modifications, we can assemble the rest here, or ship the parts and blank boards to Harvard. This is a relatively small job.

If there are an unacceptable number of modifications required for proper operation, we will have to iterate on the PCB fab, presumably in the same manner as before.

Preparation of parts orders for 5 boards: ½ day. (we scrounged parts for the 1 that is assembled).

Effort required for both boards:

Microcontroller code: 0% complete. Terry Kiper is the person for this work. I would estimate 2-3 weeks of his time to adapt code that we have on other boards these specific boards. He can probably get started sometime next week.

A VME memory map of the controller DP RAM

(Hex arithmetic has not been carefully checked)

1. Data Area (grows upward)

	Ox0: Bits 010: Leading word co	ount (word count is	s tentativel	v inclusive of itsel	f)
--	--------------------------------	---------------------	--------------	----------------------	----

-			-	<u> </u>		'				· · · ,			/			
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		N	ot Use	ed					,	WdCn	t10W	/dCnt0)			

0x2..0xN: Header Block:

0/12/10	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	04401	Dioon	,											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							TE	3D							

:

0xN+2: Data Block;

****			٠,												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Boai	rd ID							Hit Ac	ldress				

٠

0xN+0x800: End of largest possible Data Block (hit on all channels);

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Boai	rd ID							Hit Ac	ldress				

2. Control and Status Area (grows downward)

0x7FFE: Microcontroller Command Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					TE	3D						С	omma	nd cod	de

Command code list so far:

0x0: Initialize amp/disc cards

(determine # of responding boards, assign logical addresses to boards)

0x1: Write thresh block

0x2: Read thresh block

0x3: Write thresh single channel

0x4: Read thresh single channel

0x5: Write enable bits block

0x6: Read enable bits block

0x7: Write channel enable bits single card

0x8: Read channel enable bits single card

0x9: Write pipeline delays block

0xA: Read pipeline delays block

0xB Write pipeline delay single card

0xC Read pipeline delay single card

	FC: Mi	CIUCUI	ILI OIICI	Status	s (read	JOININ	11 0111	V 1V11	<i>∟)</i>							
15	14 1	3 12	2 11	10	9	8	7	6	5	4	3	2	1		()
					TBD							Busy	Comr	mand	Com	mand
													Acce	pted	Comp	oleted
0x7Fl	<i>FA:</i> Mi	crocor	ıtroller	· Board	d Cou	nt (rea	ad on	ly)								
15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
				N	lot use	ed						# c	f Res	pondir	ng Boa	ırds
0x7FI	F8: Mic	crocon	troller	Addre	ess Sp	ecifie	r (sia	nifica	ant o	nly dı	uring	single (operat	ions)		
15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
0	1				•	•	[DP R	Ram	Addre	ess	•		•	•	
0×7E	F6: Bo	ard ID	(Thie	value	ie ann	ender	d to t	ha ch	hann	اما عط	drace)				
15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
10	17	10	12	Not u		J			,					rd ID	<u>'</u>	
<u> </u>				11011	<u> </u>					Į			Воц	14 15		
TBD:																
	Son	ne nun	iber o	f word	s cont	aining	the	cons	stant	part o	of the	heade	r bloc	k		
Addre	esses t	hat fol	low wi	II need	d adius	stmen	t bv t	he n	umb	er of	words	sused	bv hea	ader ii	nforma	ition.
					•		•						.,			
	F4: Pip				1			-	<u> </u>	-				ſ	ı	1
15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
			Not i	used							Pipe	eline de	elay se	etting		
								•								
								•								
	B4: Pip				1									_		
15	14	13								6	5	4	3	2	1	0
		10	12	11	10	9	8		7	6						
		10		11 used	10	9	8		/	O		eline de	elay se	etting		ı
0x7Fl	B2: En		Not	used		9	8		/	0		eline de	elay se	etting		
0x7F 1	B2: En		Not	used		9	8		7	6		eline de	elay se	etting 2	1	0
	1	able b	Not o	used oard 0x	(0)	9	8		7	6	Pipe	4			1	0
15	1	able b	Not of the last of	used pard 0x	(0) 10 Chan	9	8		7	6	Pipe	4			1	0
15	14	able b	Not of the last of	used pard 0x	(0) 10 Chan	9	8	Bits	7	6	Pipe	4			1	0
15 0x7F	14 B0: En	able b 13 able b	Not utilits (bo	used pard 0x 11 pard 0x 11	(0) 10 Chan (0)	9 nel Er	8 nable	Bits	7 for i	6 nputs	5 15(4	3	2		
15 0x7F	14 B0: En	able b 13 able b	Not utilits (bo	used pard 0x 11 pard 0x 11	(0) 10 Chan (0) 10	9 nel Er	8 nable	Bits	7 for i	6 nputs	5 15(4	3	2		
15 0x7F 15	14 B0: En	able b 13 able b 13	Not uits (bo	pard 0x	(0) 10 Chan (0) 10 Chanr	9 nel Er	8 nable	Bits	7 for i	6 nputs	5 15(4	3	2		
15 0x7Fl 15 0x7F.	14 B0: En 14	able b able b 13	Not uits (bo	pard 0x ard 0x ard 0x ard 0x	(0) 10 Chan (0) 10 Chanr	9 nel Er	8 nable	Bits	7 for i	6 nputs	5 15(5 311	4	3	2		
15 0x7F 15	14 B0: En	able b 13 able b 13	Not uits (bo	pard 0x 11 pard 0x 11 ard 0x	(0) Chan (0) 10 Chanr 1F)	9 nel Er 9 nel En	8 able	Bits	7 for i	6 nputs 6 nputs	5 150 5 311	4 4 6 4	3	2	1	0
15 0x7Fi 15 0x7Fi 15	14 B0: En 14	able b able b 13 able b 13	Not utits (book 12) its (book 12) its (book 12)	pard 0x 11 ard 0x ard 0x	(0) Chan (0) 10 Chanr (1F) 10	9 nel Er 9 nel En	8 able	Bits	7 for i	6 nputs 6 nputs	5 150 5 311	4 4 6 4	3	2	1	0
15 0x7Fi 15 0x7Fi 15	14 B0: En 14 32: En	able b able b 13 able b 13	Not utits (book 12) its (book 12) its (book 12)	pard 0x 11 ard 0x ard 0x	(0) Chan (0) 10 Chanr (1F) 10	9 nel Er 9 nel En	8 able	Bits Bits Bits	7 for i	6 nputs 6 nputs	5 150 5 311	4 4 6 4	3	2	1	0
15 0x7F 15 0x7F 15	32: En. 14	able b 13 able b 13 able bi 13	Not units (bound 12) its (bound 12) its (bound 12) its (bound 12)	ard 0x ard 0x 11 ard 0x 11	(0) 10 Chan (0) 10 Chanr (1F) 10 Chan (1F)	9 nel Er 9 nel En 9 nel Er	8 able 8 able 8	Bits Bits	7 for i	6 nputs 6 nputs nputs	5 150 5 311	4 4 66	3 3	2 2	1 1	0
15 0x7F 15 0x7F 15	32: En. 14	able b 13 able b 13 able bi 13	Not units (bound 12) its (bound 12) its (bound 12) its (bound 12)	ard 0x ard 0x 11 ard 0x 11	(0) Chan (0) 10 Chanr (1F) 10 Chan (1F)	9 nel Er 9 nel En 9 nel Er	8 able 8 able 8	Bits Bits	7 for i	6 nputs 6 nputs nputs	5 150 5 311	4 4 66	3 3	2 2	1 1	0

15			43 (50	ard 0x	.0)										
_ , _	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Thre	shold	for Ch	an 1					Thre	shold	for Ch	nan 0		
								-							
		reshol	•			Π	1			1	1		1	Ι	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Thres	shold f	or Cha	an 31					Thres	shold 1	for Ch	an 30		
								•							
0x7B	2<i>E:</i> T h	reshol	lds (bo	ard 0x	(1F)			•							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	l	Thre	shold	for Ch	an 1	l	l			Thre	shold	for Ch	an 0		
		resho			(1F)	Т	1			_	1	_	1		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Thres	shold f	or Cha	an 31					Thres	shold t	for Ch	an 30		
The fe							ا ا) /-f -	41					
ine io	ollowin	g valu	es are	updat	ea pe	riodica	ally by	tne uc	, (OI O	raer 11	HZ)				
The following values are updated periodically by the uC (of order 1Hz) 0x7B0C: Power supply readback (board 0x0)															
0x7B	0 C: Po	wer s	upply i	readba	ack (bo	oard 0	x0)								
0x7B 15	0C: Po	wer s	upply i	readba	ack (bo	oard 0:	x0)	7	6	5	4	3	2	1	0
	14		12	11	10	9		7		5 Supply					0
	14	13	12	11	10	9		7							0
15	14 -5 \$	13 Supply	12 Value	11 e (40 m	10 nV/Co	9 unt)	8	7							0
15 0x7A	14 -5 \$ EC: Po	13 Supply	12 Value upply	11 e (40 m	10 nV/Cor ack (be	9 unt) oard 0	8 x1F)		+5	Supply	y Valu	e (40n	nV/Co	unt)	
15	14 -5 \$ EC: Po	13 Supply ower s	12 Value upply 12	11 e (40 m readba	10 nV/Cor ack (be	9 unt) oard 0	8	7	+5	Supply 5	y Valu	e (40n	nV/Cor	unt)	0
15 0x7A	14 -5 \$ EC: Po	13 Supply	12 Value upply 12	11 e (40 m readba	10 nV/Cor ack (be	9 unt) oard 0	8 x1F)		+5	Supply	y Valu	e (40n	nV/Cor	unt)	
15 0x7A 15	14 -5 \$ EC: Po 14 -5 \$	13 Supply ower s	12 Value upply 12 Value	11 readba 11 e (40 m	10 nV/Con ack (be 10 nV/Con	9 unt) oard 0 9 unt)	x1F) 8	7	+5 6 +5	Supply 5	y Valu	e (40n	nV/Cor	unt)	
15 0x7A 15	14 -5 \$ EC: Po 14 -5 \$	13 Supply ower s 13 Supply	12 Value upply 12 Value	11 readba 11 e (40 m	10 nV/Con ack (be 10 nV/Con	9 unt) oard 0 9 unt)	x1F) 8	7	+5 6 +5	Supply 5	y Valu	e (40n	nV/Cor	unt)	
0x7A 15 0x7A	14 -5 \$ EC: Po 14 -5 \$ EA: Ar	Supply ower s 13 Supply mbient	12 Value upply 12 Value tempe	11 readba 11 e (40 m	10 nV/Con ack (be 10 nV/Con	9 unt) oard 0 9 unt)	x1F) 8 pack (t	7 poard (+5 6 +5 0x0) 6	Supply 5 Supply	y Valu 4 y Valu	e (40n	2 nV/Co	unt) 1 unt)	0
0x7A 15 0x7A	14 -5 \$ EC: Po 14 -5 \$ EA: Ar	Supply ower s 13 Supply mbient	12 Value upply 12 Value tempe	11 readba 11 e (40 m	10 nV/Con ack (be 10 nV/Con	9 unt) oard 0 9 unt)	x1F) 8 pack (t	7 poard (+5 6 +5 0x0) 6	Supply 5 Supply	y Valu 4 y Valu	e (40n	2 nV/Co	unt) 1 unt)	0
0x7A 15 0x7A 15	14 -5 \$ EC: Po 14 -5 \$ EA: Ar	Dwer s 13 Supply Dwer s 13 Supply mbient 13	12 Value upply 12 Value tempe	readba 11 e (40 m	10 nV/Con 10 nV/Con 2 ADC	9 unt) oard 0 9 unt) readb	x1F) 8 pack (b 8 °C =	7 ooard (7 (ADC (+5 6 +5 0x0) 6 Count	Supply 5 Supply	y Valu 4 y Valu	e (40n	2 nV/Co	unt) 1 unt)	0
0x7A 15 0x7A 15	14 -5 \$ EC: Po 14 -5 \$ EA: Ar 14	13 Supply ower s 13 Supply mbient 13	12 Value upply 12 Value tempe 12	readba 11 e (40 m erature 11 erature	10 ack (be 10 nV/Con 10 nV/Con 10 10	9 unt) oard 0 9 unt) readb	x1F) 8 pack (b °C = c	7 poard (7 (ADC (+5 6 +5 0x0) 6 Count	Supply 5 Supply 5 s - 16	y Valu 4 y Valu 4 15) · 0	3 e (40n	2 nV/Con 2	unt)	0
0x7A 15 0x7A 15	14 -5 \$ EC: Po 14 -5 \$ EA: Ar	Dwer s 13 Supply Dwer s 13 Supply mbient 13	12 Value upply 12 Value tempe	readba 11 e (40 m	10 nV/Con 10 nV/Con 2 ADC	9 unt) oard 0 9 unt) readb	x1F) 8 pack (k 8 °C = (b	7 poard (7 (ADC (+5 6 +5 0x0) 6 Count 0x1F) 6	Supply 5 Supply	4 y Valu 4 y Valu 4 15) · 0	3 e (40n	2 nV/Co	unt) 1 unt)	0

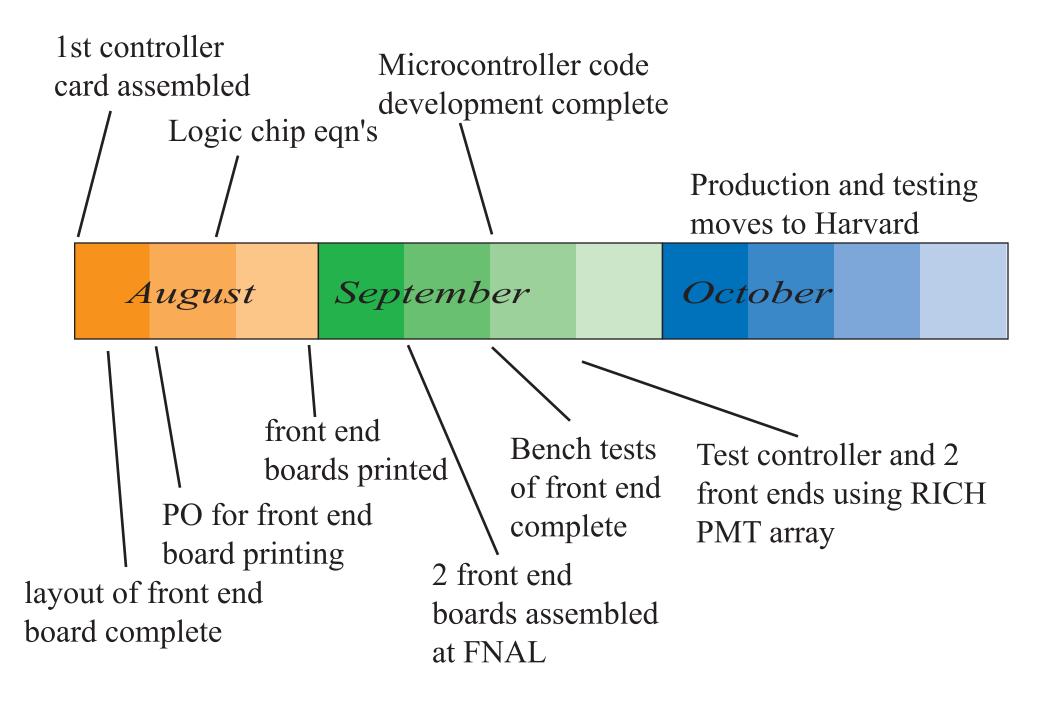
Notes:

The starting address for each data type in the control section of the RAM area is fixed. The significant length of each block is dependent on the number of active cards in the control chain.

Front End Board Testing

- Power PC loaned to Harvard by LNL in May
- Andre L. has kernal and file system built and working
- Waiting for controller card to play with
- Andre (and Sharon?) will write testing code
- This code will be re-used in the DAQ for the RICH

Plan For RICH Electronics



RICH HV

- HV supplies in SELEX portacamp. 7 of 8 power up
- located SELEX HV manual
- Interupt system works and I think I understand it

- Andre has looked
into a few other
options:

Power Supply	HV(kV)	Current (mA)	Price(\$)
Bertan			
102-02	2	500	4,000 x 6
102-03	3	333	4,000 x 6
Glassman			
PS/EW02R300-1	15 2	300	2,300 x 6
PS/EK02R300-11	5 2	300	2,300 x 6
CAEN	2.5	13/chan	45,600
Matsuada			
AU-3	3	200	3,100 x 6
AU-2	2	300	3,100 x 6
W	350 V	Vatts	1,000 x 6

RICH MC Work

Sharon S. has imported code from SELEX for RICH hits as well as digitization code to MIPP Monte Carlo

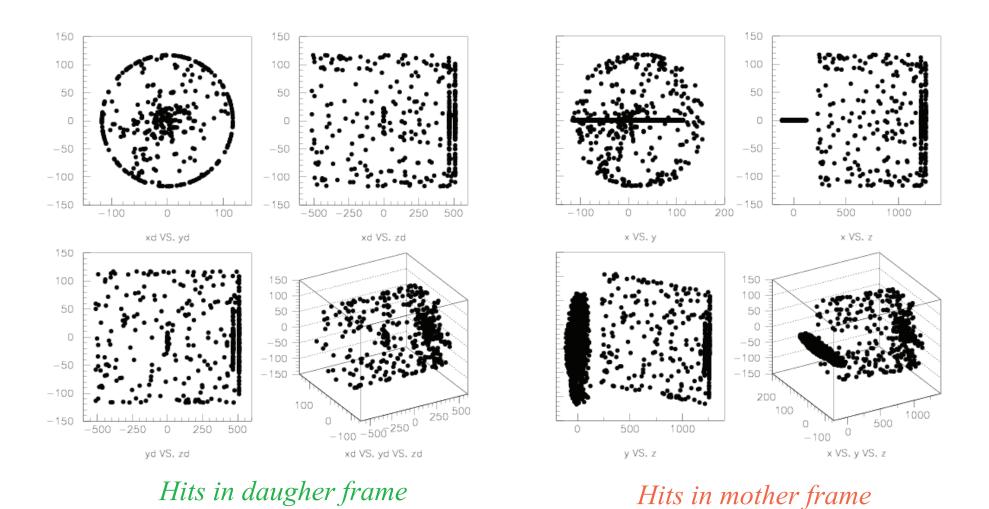
All compiles, links, and runs, but...

Results don't look right. Most likely a bug in the hit packing.

Sharon takes her oral qualifying exam next week and will get back to working on the code. Hope to make study of CO2 by middle of September

Sharon also has SELEX reconstruction code in hand and has begun to understand how it works. Probably easiest to rewrite this once the algorithms are understood. Might be easier just to check $\pi/K/p$ hypotheses rather than fit ring radii.

RICH Hits



To me, looks like error in hit packing...

(Sharon Seun)

Calling sequence for SELEX reconstruction code

